

1. A scan test system for a semiconductor device,  
comprising:

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6. A scan test system for a semiconductor device according to Claim 4, wherein the switching means comprises: a first switch, a first bypass line that bypasses the first register chain, a second switch and a second bypass line that bypasses the second register chain, the first switch switches between the first register chain and the first bypass line, and the second switch switches between the second register chain and the second bypass line.